The Parallel Architectures research Group (GAP) of the Polytechnic University of Valencia has a long experience working on interconnection networks for parallel computers, ranging from large supercomputers, through clusters of personal computers, usually used as servers, to the networks on chip in multicore processors. GAP has also developed research in related subjects, such as, processor microarchitecture and the cache coherence protocols. During the last eighteen years, this research has been supported by six CICYT National grants, although it began previously.

In the field of interconnection networks, all the topics related to networks, such as new topologies definition, new switching techniques, new unicast and multicast routing algorithms, both determinist and adaptive, as well as more efficient strategies for traffic balancing, congestion control and fault tolerance, are being practically approached. The GAP has also worked in the design of high performance and low cost multimedia switches, and new designs for routing hardware, for both off-chip and on-chip. Finally, new statistical techniques have also been introduced to improve the network evaluation process.

The general mission of GAP is to develop applied research of quality, but under realistic hypotheses and considering the market trends, so that enables technology transfer to the industry. This proved effective with the development of fully adaptive routing algorithms in experimental parallel machines (Reliable Router of the Massachusetts Institute of Technology) as well as in commercial machines (Cray T3E of Cray Research Compaq Alpha 21364). More recently, these techniques have been used in the design of IBM BlueGene/L supercomputer (the supercomputer which has headed the Top500 list, the four years, until June of 2008).

Other remarkable hits of the group, measured by their impact in the industry, are the development of very efficient determinist routing algorithms for multistage networks, the development of very compact and versatile routers for networks on chip, and the development of efficient techniques for congestion control. Regarding to the first result, Sun Microsystems has implemented a partitionable version of this algorithm in its Magnum switch, which is the largest switch for InfiniBand at present (3456 ports), and it has been used, among others, in the Ranger supercomputer, that occupied the fourth place of the Top500 list in June of 2008. The second result has been developed in collaboration with AMD; proposing solutions for all the requirements of networks on chip that AMD anticipates for their future processors, so having good perspectives for its practical application. The third result was developed in collaboration with Xyratex, it was patented, and the standardization process of these congestion control techniques began, denominated RECN, like part of the specifications of Advanced Switching Interconnect (ASI). Unfortunately, the Consortium ASI disappeared before the standardization was completed.
GAP has been one of the pioneer groups at international level, regarding the research of commercial networks switches (InfiniBand, Quadrics, ASI). In summary, the GAP proposed the first strategies to implement the routing tables in InfiniBand and several routing techniques designed for network load balancing, including some enhancements to use adaptive routing, not originally supported in the standard. It also developed efficient techniques to allow collective communications in the Quadrics network, in those cases in which the set of destination nodes was not a range of consecutive directions. Additional examples are routing techniques for InfiniBand, implanted in the Switch Magnum of Sun Microsystems, and congestion control techniques (RECN) for ASI, already mentioned previously.

But the main achievement in this field has been the development and standardization of new HyperTransport specifications, in which the number of addressable devices in the network extends, passing from the previous value of 32 to the present one of 4 billion, and defining the new communication protocol and the packet format for this extension, while the compatibility with the previous standard remains. This standarization process has been complex, as supposed to convince companies like AMD, Hewlett-Packard and Sun Microsystems to assume drastic changes in their servers’ architecture, varying from distributed memory architecture to a shared memory, and also how this type of architecture was going to have a commercial demand. At present, Universitat Politècnica de Valencia is member of the HyperTransport Consortium, in which has been constituted the Advanced Technology Group (ATG); this group is led by the main researcher in GAP, and has developed compatible extensions to the HyperTransport specifications, approved by the HyperTransport Consortium.

In addition, our group has strong collaboration links with several European research groups (Simula Research Laboratory in Oslo, University of Heidelberg, University of Ferrara, University of Catania), the United States (Georgia Institute of Technology, University of Southern California, University of Illinois at Urban, Ohio State University, Pennsylvania State University, Los Alamos National Lab., Princeton University) and Japan (Keio University), as well as with different companies with cutting-edge technology (IBM, Sun Microsystems, Intel, AMD, Xyratex, Quadrics). The members of our research team have been coauthors of more than 100 articles with researchers from American, European and Asian universities. Also we have filled joined patents with the research laboratory of IBM in Zurich; with Xyratex, British company, and with ST Microelectronics.

These research works have been published in the best journals (IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, Journal of Parallel and Distributed Computing, Journal of Systems Architecture, etc.) and international conferences (International Symposium on Computer Architecture, High Performance Computer Architecture,
International Conference on Parallel Processing, IEEE Parallel and Distributed Processing Symposium, Parallel Architectures and Languages Europe, EuroPar, etc.). Some of those works have been mentioned more than 500 times, according to Google Scholar.

Our group is an international reference in the field of interconnection networks. Several members of the group have been invited in numerous occasions for program committees of the most prestigious international conferences in our research field, being editors and associated editors also in IEEE TPDS, IEEE TC, IEEE CAL and Parallel Computing. The research leader has chaired program committee of conferences like HPCA-10 and ICPP2005, delivering as well several keynotes in different major conferences and Universities in the United States.

The state-of-the-art on the interconnection networks has shaped in the titled book "Interconnection Networks: An Engineering Approach", published by Morgan Kaufmann. This book has been written by the main researcher of the group, with the collaboration of professors Sudhakar Yalamanchili (Georgia Institute of Technology) and Lionel Ni (Michigan State University), and is being used to teach in several universities of the United States. This book counts with more than thousand references in Google Scholar. Also, the main researcher is co-author, along with professor Timothy Pinkston (University of Southern California), of the appendix on interconnection networks published in the fourth edition of the book "Computer Architecture: a Quantitative Approach", of John Hennessy and David Patterson, which is the reference book in this topic.

For the network-on-chip research, members of the research group have coauthored and edited a recent book for the subject: Designing Networks-on-Chip Architectures in the Nanoscale Era, which reflects most of the current state-of-the-art research in the field of on-chip interconnects.